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REMARKS

Claims 1-30 are pending. Claim 21 was objected to under 37 CFR 1.75 (c) as being an improper dependent claim. Claim 21 has been amended to address this objection. Claim 7 was objected to under 35 U.S.C. 112 as having terms with insufficient antecedent basis. Claim 7 has been amended to overcome this objection. The Examiner objected to claims 1-13 under 35 U.S.C. 112(2) as being indefinite because of the phrase in independent claim 1 "substantially all multi-byte aligned branch instructions." The language in independent claim 1 and the use of the term "substantially" is believed proper. According to MPEP 2173.05(b) paragraph D, "The term "substantially" is often used in conjunction with another term to describe a particular characteristic of the claimed invention. It is a broad term. *In re Nehrenberg*, 280 F.2d 161, 126 USPQ 383 (CCPA 1960). The court held that the limitation "to substantially increase the efficiency of the compound as a copper extractant" was definite in view of the general guidelines contained in the specification. *In re Mattison*, 509 F.2d 563, 184 USPQ 484 (CCPA 1975). The court held that the limitation "which produces substantially equal E and H plane illumination patterns" was definite because one of ordinary skill in the art would know what was meant by "substantially equal." *Andrew Corp. v. Gabriel Electronics*, 847 F.2d 819, 6 USPQ2d 2010 (Fed. Cir. 1988).

Independent claim 1 was rejected under 35 U.S.C. 102(b) as being anticipated by Intel (IA-32® Architecture Software Developer's Manual, Volumes 1-2, 2002). Independent claim 1 recites "wherein substantially all multi-byte aligned branch instructions are operable to access the instructions at byte aligned addresses." The Examiner cites multiple jump instructions listed on page 3-357. The jump instructions include JMP rel8, JMP rel16, JMP rel32, JMP r/m16, JMP r/m32, JMP ptr16:16, JMP ptr16:32, JMP m16:16, and JMP m16:32. The Examiner argues that these jump instructions are operable to access the instructions at byte aligned addresses.

The Applicants respectfully disagree. Intel in fact describes only a single jump instruction, JMP rel8 that is operable to access the instructions at byte aligned addresses. All of the other listed jump instructions, a total of eight out of nine, are operable to access the instructions only a multi-byte aligned addresses. The specification of the present application clearly describes a byte aligned address. "Any instruction having a start address at any byte address is referred to herein as a byte aligned instruction." (page 6, lines 16-17) The Intel JMP

16 and JMP 32 instructions do not allow access to instructions having a start address at any byte address. In fact, they only allow access to instructions at multi-byte addresses, for example, multiples of 16 and 32. Consequently, Intel does not teach or suggest "wherein substantially all multi-byte aligned branch instructions are operable to access the instructions at byte aligned addresses."

In fact Intel is believed to describe the prior art mentioned in the specification. "Many of the conventional processors are being configured to support smaller instructions. In many cases, new branch instructions are being written simply to handle these particular smaller instructions. The conventional processors are consequently left with different groups of branch instructions. One group of branch instructions handles 16-bit aligned instructions. Another group of similar branch instructions handles 8-bit aligned instructions. These redundant groups of branch instructions in conventional processors are highly inefficient." (page 8, lines 10-17)

Independent claim 14 recites "common subcircuitry is used to process the immediate field associated with one or more branch instructions and one or more non-branch instructions" and independent claims 20 and 27 recite "common subcircuitry operable to calculate a byte-aligned address, wherein the common subcircuitry is also configured to perform nonbranch operations." Intel does not describe common subcircuitry recited in the independent claims 14, 20, and 27. The Examiner argues that the common subcircuitry is inherent. The Applicants respectfully disagree. Intel does not teach or suggest or otherwise describe any common subcircuitry because Intel only describes a conventional IA-32 processor, which uses different groups of branch instructions and different circuitry to handle 8-bit versus 16-bit versus 32-bit instructions. As noted in the present specification, "one group of branch instructions handles 16-bit aligned instructions. Another group of similar branch instructions handles 8-bit aligned instructions. These redundant groups of branch instructions in conventional processors are highly inefficient." (page 8, lines 15-17)

CONCLUSION

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Godfrey K. Kwan
Reg. No. 46,850

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100